Features

- Fully computer controlled
- 14-bit fixed conversion time ADC
- DNL enhancement circuit
- Fast processing time <600ns
- Selectable input voltage range: 2.5v, 5v, 10v
- Multi-Channel Scaler (MCS) functionality
- Peripheral I/O control
- Alternate MCS functionality
- Suitable for SDD, NaI(Tl), HPGe and other detector technologies
- Ethernet, USB, RS232 or RS485 communications interfaces

Description

The ADC/MCA is a state-of-the-art, high performance PHA processor combined with a Multi-channel Analyzer. It is intended for use in systems, where existing shaping amplifiers require high performance analog signal processing and spectra capturing. The industry standard interface options provide users with great flexibility at low cost.

A variety of options ranging from OEM modules to ready-for-use stand-alone devices are available.

The small footprint makes this device ideal for portable applications, as well as for customer-specific installations.

The ADC/MCA is fully supported by our SpectLab software. Software specifications are available to potential developers.

Specifications

ADC INPUT – accepts positive unipolar pulses for PHA with amplitude 0-5V (default), 0-2.5V, 0-10V. Other ranges are possible on request. Rise time >300ns, pulse width > 600ns, Z = 1kΩ. Coupling: BNC or Lemo 00 series connector.

PUR/TRIGGER – TTL/LVTTL input level. Coupling: BNC or Lemo 00 series connector.

GATE – TTL/LVTTL input level. Enable / disable module operation. Forced low by 10kΩ pull-down resistor. Polarity selected through software. Coupling: 2mm pitch plug.

D_T – TTL/LVTTL input level. External dead time signal input. Active high. Forced to inactive state by 10kΩ pull-down resistor. Coupling: 2mm pitch plug.
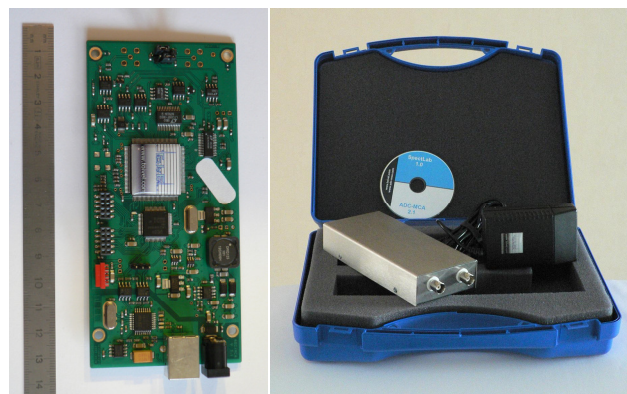
SCK, SDI, SDO – TTL/LVTTL 3-wire serial interface clock and data. Used to control user-specific features of front-end electronics. Coupling: 2mm pitch plug.

I/O 0..7 – TTL/LVTTL user-specific I/O signals. Coupling: 2mm pitch plug.

AN_0 – 0-2.5v range user-specific analog input. Coupling: 2.54mm pitch connection (J16).

+3.3v, GND – power output for external logic. 100mA max. Coupling: 2mm pitch plug.

Software controls
ADC LLD – 0 to 100% of full scale. 4096 levels.
ADC ULD – 0 to 100% of full scale. 4096 levels.
ADC D_T – 0 to 100% of full scale. 4096 levels.
ADC conversion range – 512, 1024, 2048, 4096, 8192 channels.
Real time preset – up to 2^{32} sec.
Live time preset – up to 2^{32} sec.
MCS dwell time – 480ns to 2^{29} sec.

Communication
USB – Standard USB port using type B connector.
ETHERNET – Optional Ethernet port using TCP/IP, replaces USB interface.
RS485/RS232 – Optional.

Performance
INTEGRAL NONLINEARITY – < 0.1%
DIFFERENTIAL NONLINEARITY – < 0.5%
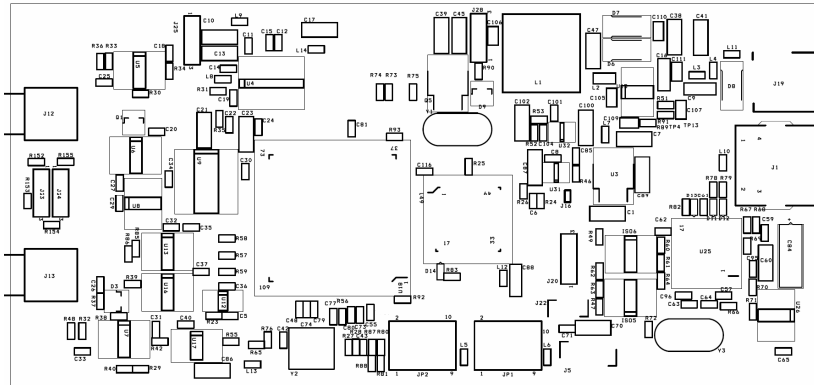ADC+MCA DEAD TIME – 600ns after peaking time

Power consumption
When USB powered only: + 5V, 380mA.
When dual powered: + 12V, 180mA, +5V, 70mA from USB.

Dimensions
130 x 60 x 20 mm (PCB module)
150 x 70 x 30 mm (stand-alone, in metal housing)

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JP1 pinout.

Contact number	Signal name	Comment
1	GND	Ground connection
2	SCK	3-wire serial clock, LVTTL
3	FRAME	LVTTL
4	SDO	3-wire serial data out, LVTTL
5	IO4	LVTTL
6	IO5	LVTTL
7	IO6	LVTTL
8	IO7	LVTTL
9	VCC	+3.3V
10	GND	Ground connection

JP2 pinout.

Contact number	Signal name	Comment
1	GND	Ground connection
2	D_T	LVTTL
3	GATE	LVTTL
4	IO0	LVTTL
5	IO1	LVTTL
6	IO2	LVTTL
7	IO3	LVTTL
8	SDI	3-wire serial data in, LVTTL
9	VCC	+3.3V
10	GND	Ground connection

J19 pinout.

Contact number	Signal name	Comment
1 (central)	+12V	+12V power supply
2 (shell)	GND	Ground connection

J23/J24 input range selection. Jumper positions.

J23	J24	Range
1-2	1-2	0-10V, Z=1k
2-3	1-2	**0-5V, Z=1k; default setting**
2-3	2-3	0-2.5V, Z=1k

Block Diagram

USB*'**

Ethernet
UTP*

CPU control

MCA Memory

ADC 4k/8k

Input from
Shaping Amplifier
5V peak (optional 2.5,10V)

12V DC from
external power
supply **

Power supply
+/-5V, 3.3V

Control logic

Peak
detector

LLD, ULD, DTD
DAC's

LLD, ULD, DTD
comparators
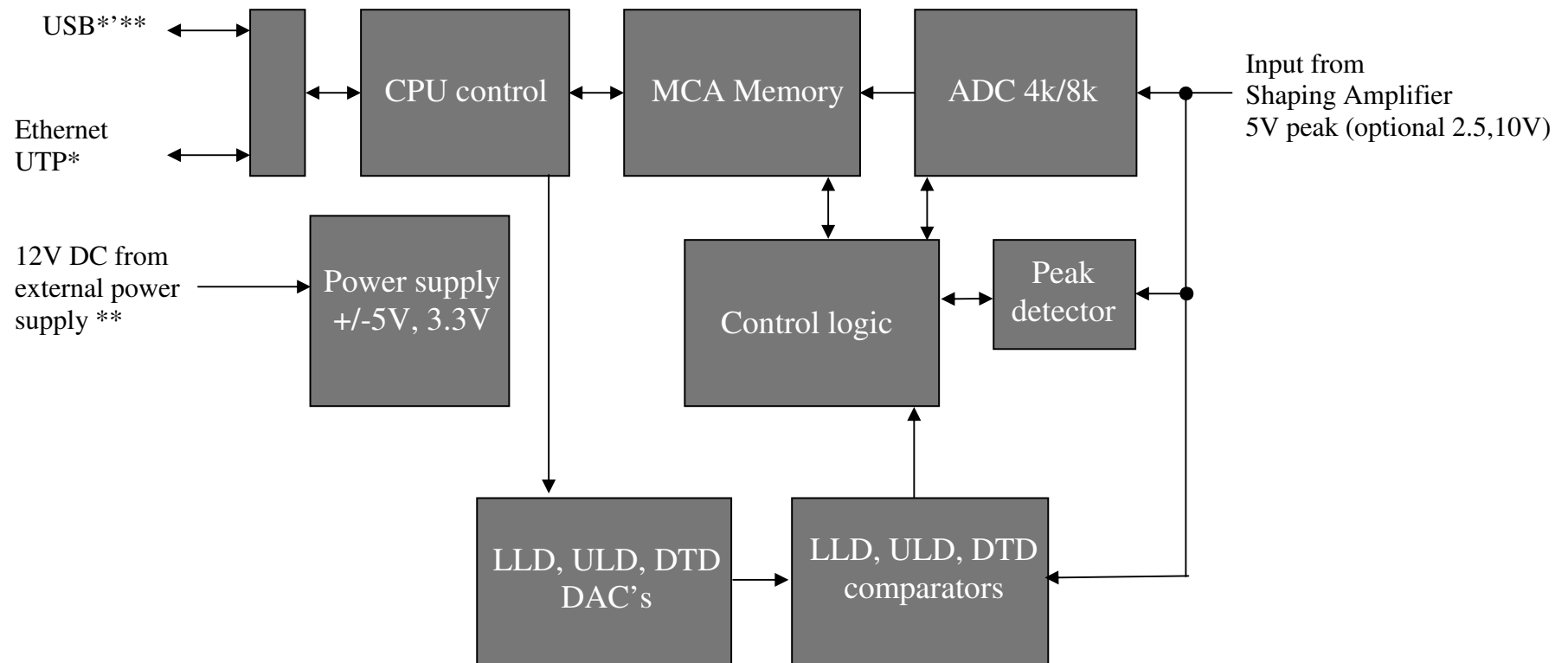
* Depending on interface option
** USB power supply possible

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